A NOVEL WHISKERLESS SCHOTTKY DIODE FOR MILLIMETER AND SUBMILLIMETER WAVE APPLICATION

Q-16

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Abstract

A novel whiskerless Schottky diode has been developed in which shunt capacitance is minimized by means of an etched surface channel. This structure is easily fabricated and the DC I-V characteristics are as good as those of the best available whisker-contacted devices. Preliminary RF characterization in an unoptimized mount at 110 GHz has yielded room temperature SSB mixer noise temperature of 950 K and SSB conversion loss of 6.4 dB. The diode is robust and can be operated at cryogenic temperatures. Potential applications include waveguide and planar mixers, planar arrays, multipliers, varactor tuners, and microwave integrated circuits.

Introduction

Schottky barrier diodes with anode diameters in the submicron to micron range are widely used as resistive mixer elements and varactor multipliers at high frequencies (100 GHz to 3 THz). The requirements of extremely low shunt and junction capacitances severely restrict diode design from the standpoint of epitaxial layer thickness, doping density and contact lead geometry. The basic whisker-contacted diode arrangement (Figure 1) consists of a small GaAs chip with a close packed array of Schottky anodes which are contacted with a fine, pointed wire (whisker). This structure has long been used to satisfy the need for minimum shunt capacitance. The whisker also provides tuning inductance which can be varied by changing its shape and length.

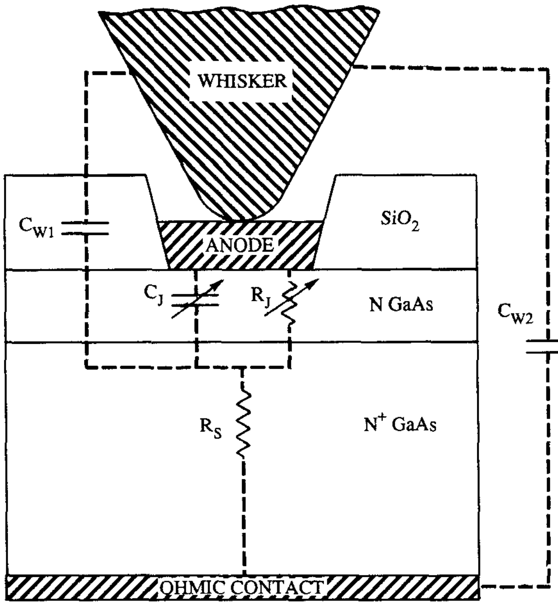

Figure 1. Whisker-Contacted Schottky Diode

Total shunt capacitance from the whisker is on the order of 1 fF and zero bias junction capacitance values as low as 0.7 fF have been achieved in this laboratory [1], [2]. Of the two shunt components, the capacitance C_{W1}, is most detrimental to high frequency performance since it is within R_S and is thus very difficult to tune out. Capacitance C_{W2}, on the other hand, can be largely tuned out with an external inductance.

Whisker-contacted diodes have a number of serious disadvantages. They are sometimes mechanically unstable in high vibration environments, such as a rocket launch, and cryogenic operation requires special mount designs to maintain whisker contact as the various elements change dimension on cooling. Also, whiskered diodes are virtually impossible to incorporate into integrated circuitry, such as diode arrays or integral antenna schemes and small area diodes (< 1 micron) require great skill and effort to contact.

Whiskerless Schottky diodes which eliminate some or all of these problems have been proposed and/or fabricated by many laboratories [3]-[10]. The basic structure is shown in Figure 2. C_P and C_F are the parallel

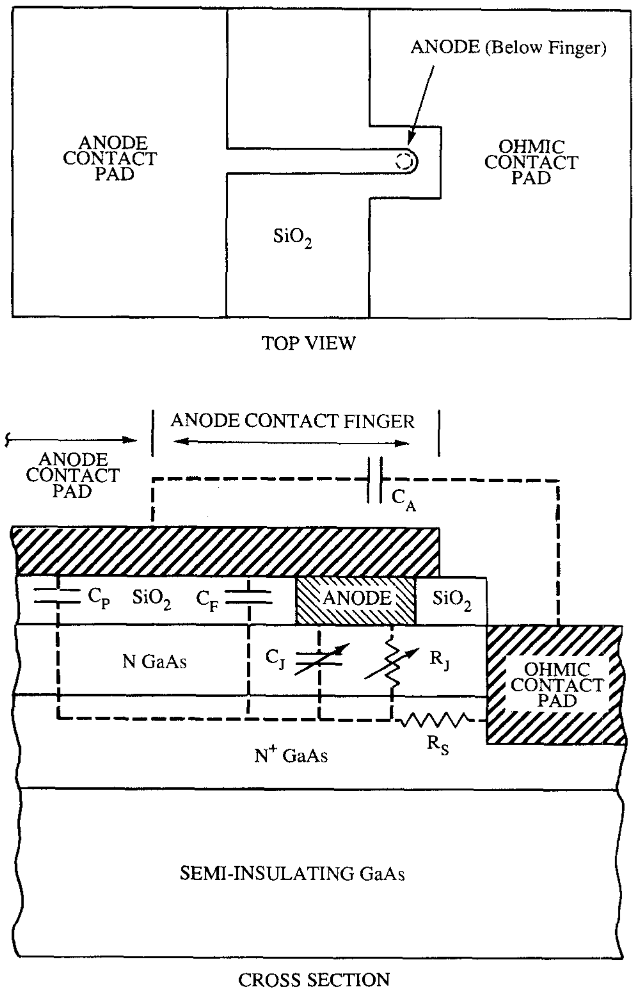

Figure 2. Basic Whiskerless Schottky Diode

plate capacitances from the anode contact pad and the anode contact finger, respectively, to the underlying gallium arsenide. C_A is due to the fringing field above the chip from the anode contact pad and finger to the ohmic contact pad. For reasonable pad dimensions (e.g., 125 x 125 microns), C_P is relatively large (1 pF) compared to C_F or C_A and can be only partially eliminated by standard beam-lead technology. This capacitance is very detrimental since it is connected within the series resistance, R_S.

Several methods to reduce or eliminate this major source of shunt capacitance have been proposed. In the mesa structure (Figure 3), the active gallium arsenide is etched away and the anode contact pad is formed over semi-insulating material. This technique is difficult to implement because of processing problems encountered in depositing and etching photoresist, oxide and metal layers on a non-planar surface. These problems are exacerbated by the precise control needed to produce very small anode diameters.

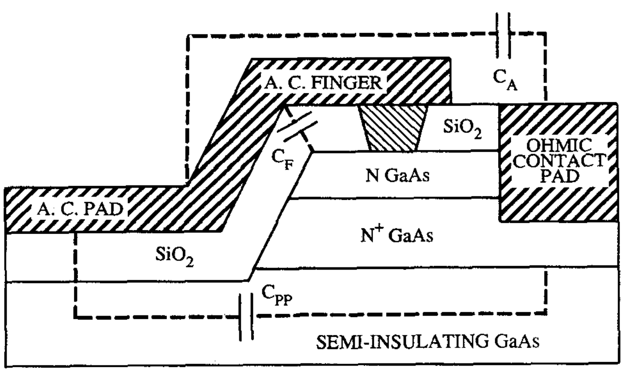

Figure 3. Mesa Structure Whiskerless Diode

In the proton-bombarded structure (Figure 4), a proton beam is used to convert the gallium arsenide beneath the anode contact pad and finger to semi-insulating material, thus eliminating the need for a mesa. The disadvantage of this method is the need for high energy proton sources for complete conversion of the thick (3 to 4 micron) degenerately doped buffer layer, and the additional photolithographic and metallization steps needed to protect the anode and ohmic contact areas from the proton beam.

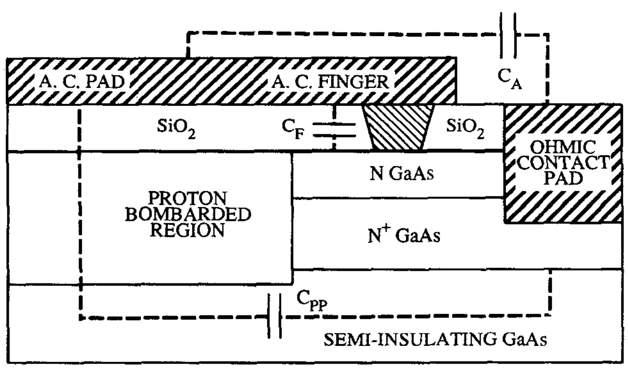

Figure 4. Proton Bombarded Whiskerless Diode

It should be emphasized, that in both of these structures, the shunt component, C_P, is replaced by C_{PP}, which is due to the fringing field between the pads through the dielectric (GaAs). This capacitance can be on the order of 10 to 20 fF. It can be minimized by reducing pad area, increasing pad separation, reducing the thickness of the dielectric, or providing a material with lower dielectric constant under and between the pads. However, this capacitance lies outside R_S and thus presents less of a problem since it can be tuned out with external inductance.

The New Whiskerless Diode Structure*

A new whiskerless diode structure has been developed at the Universty of Virginia which achieves both low junction and shunt capacitance in a structure which is relatively simple to fabricate. This design incorporates a novel "air bridge" which effectively eliminates the shunt capacitance, C_P, of Figure 2.

The structure is illustrated in Figure 5. A narrow groove, or "surface channel", is etched through the active gallium arsenide and into the semi-insulating substrate completely across the width of the chip and under the anode contact finger. This channel effectively cuts off the current path from the capacitance C_P to the anode. Remaining shunt capacitance is primarily due to the relatively small fringing field component, C_{PP}, between the contact pads, in series with C_P.

Following a method given by Ohta, et al, a value of approximately 15 fF is expected for the total pad-to-pad capacitance for the pad dimensions of the prototype device [11]. Parallel plate capacitance, C_F, for the portion of the finger overlying active gallium arsenide is approximately 2 fF. This value can be minimized by placing the edge of the surface channel as close as possible to the anode.

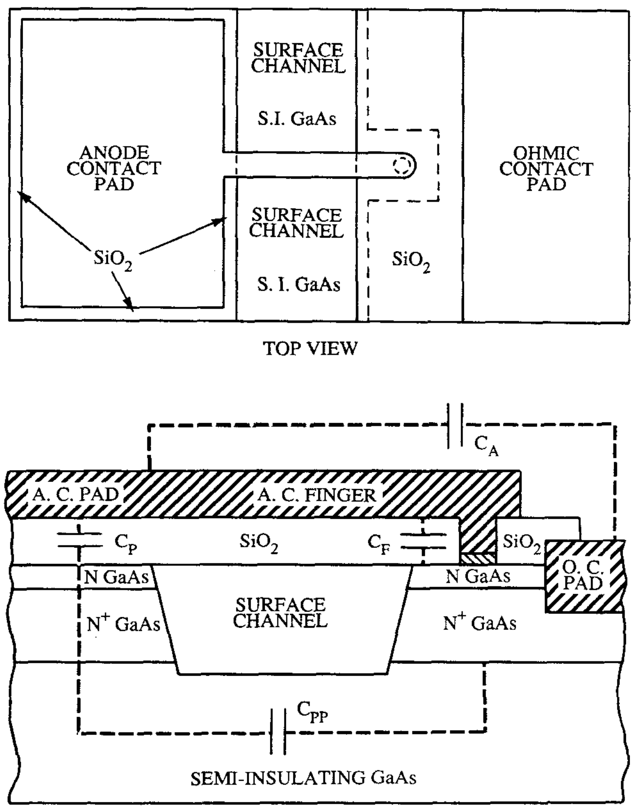

Figure 5. Surface Channel Schottky Diode

* A patent application for this device structure is underway through NASA under contract NS5-24218.

Diode Design and Fabrication

A prototype surface channel structure designed for room temperature operation and designated with batch number SC2R1 was fabricated as follows:

1. Epitaxial GaAs wafer with semi-insulating substrate (lightly Cr doped), 3.5 μm buffer layer (>$2\times10^{18}/cm^3$), 0.1 μm active layer ($2\times10^{17}/cm^3$);
2. Silicon dioxide deposition to a thickness of 5000 Å using atmospheric pressure CVD with silane at 350 °C;
3. Ohmic contact definition using patterned photoresist followed by wet etching (BHF) of the silicon dioxide;
4. Ohmic contact formation with electroplated tin/nickel, nickel, and gold which is alloyed and overplated with gold;
5. Silicon dioxide deposition to a thickness of 2000 Å using atmospheric pressure CVD with silane at 300 °C;
6. Anode window definition for a 2.5 μm anode using patterned photoresist followed by wet etching (BHF) of the silicon dioxide;
7. Anode formation with electroplated platinum followed by gold;
8. Sputter deposition of 600 Å of chromium followed by 1000 Å of gold over the entire wafer surface;
9. Anode contact definition with photoresist followed by 3 μm of plated gold to form the contact pad and finger;
10. Removal of the sputter deposited gold and chromium around the contact pad and finger with sputter etching and wet chemical etching ($KMnO_4$:NaOH).
11. Surface channel definition using patterned photoresist followed by wet etching of the silicon dioxide (BHF).
12. Surface channel formation using wet chemical etching (NaOH:H_2O_2) of the gallium arsenide.
13. Removal of silicon dioxide from the ohmic contact pad using patterned photoresist and wet etching (BHF).
14. Dicing and testing.

A very important feature of the fabricaton process is the fact that the surface channel is formed at the end of the sequence. The critical processing steps of ohmic contact formation, anode formation and contact pad/finger formation are thus carried out on a planar surface.

A scanning electron micrograph of a completed surface channel device is shown in Figure 6 (The chip is mounted with silver paint to the SEM specimen holder). The chip is about 390 μm long, 130 μm wide and 130 μm thick. The anode contact pad is approximately 100 μm wide and 200 μm long with a 3 μm x 50 μm long finger projecting across the surface channel to the anode. The surface channel in the prototype also encircles the anode contact pad to facilitate dicing. Future devices will be fabricated with the simple transverse channel shown in Figure 5. The ohmic contact pad is approximately 130 μm square. The chip can be soldered or bonded to the microwave circuit.

Results and Discussion

The electrical characteristics of the surface channel device structure are summarized in Table I. Series resistance and junction ideality values are as low as those of the best conventional whisker-contacted diodes fabricated in this laboratory on similarly doped epitaxial material. Breakdown voltage and zero-bias capacitance are predicted by epi layer doping and thickness and anode diameter. Although these devices were designed for room temperature application, diodes cooled to 77 K exhibited a reduction of ΔV to 35 mV without degradation. This demonstrates that the structure is mechanically stable at cryogenic temperatures and no special temperature compensation is required in diode mounting.

Junction and shunt capacitance values were determined experimentally by measuring the capacitance of both working chips and that of open circuits which were identical to the working devices except that the anodes were omitted during fabrication (i.e., both the anode contact pad and finger were intact). This shunt capacitance, which is inherent in all planar diode designs, is due largely to the fringing field between the contact pads through the gallium arsenide substrate. It should be possible to tune out this element of shunt capacitance with an external inductance or to incorporate it into the waveguide or antenna structure.

The surface channel device was RF tested at 110 GHz by mounting it across a reduced height waveguide (type WR-8 waveguide mount). In this unoptimized system, the room temperature SSB mixer noise temperature was 950 K and SSB conversion loss was 6.4 dB. This noise performance is within approximately a factor of two of the best reported results for a room temperature mixer using conventional whisker-contacted diodes in an optimized mixer [12]. These results are most encouraging.

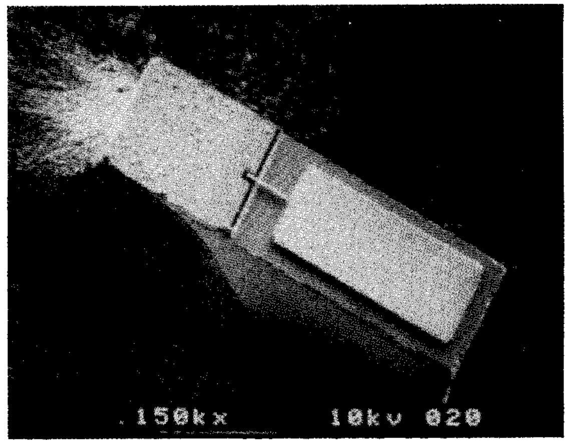

Figure 6. SEM of the Surface Channel Diode

Table I
Electrical Characteristics of Surface Channel Schottky Diodes

Diode Type	Room Temperature Mixer
Anode Diameter	2.5 μm
ΔV(10-100 μA)@295 K	71-72 mV
Ideality @ 295 K	1.2
ΔV(10-100 μA) @ 77 K	34-35 mV
R_s @ 295 K	5-6 ohms
V_{bR} (1 μA)	4.5-5.5 volts
C_{jo}	5-6 fF
C_{shunt}	13-15 fF
SSB Mixer Noise Temperature, 110 GHz	950 K
SSB Mixer Conversion Loss, 110 GHz	6.4 dB

Conclusions

A robust, high quality, easily fabricated whiskerless Schottky diode has been developed in which shunt capacitance is minimized with a simple etched surface channel. The device should find numerous applications in the millimeter and submillimeter field, including use as:

1. waveguide mixers,
2. planar mixers and planar arrays,
3. multipliers,
4. varactor tuners, and
5. microwave integrated circuits

The focus of whiskerless diode research at the University of Virginia is to develop device structures to satisfy the following general goals:

1. DC I-V characteristics at least equal to that of the best available whisker-contacted diodes.
2. Minimum shunt and junction capacitance.
3. RF performance at least equal to the best available whisker-contacted diodes.
4. Suitable for both room temperature or cryogenic operation.
5. Robust design suitable for high-vibration environments.
6. Easy bonding or soldering to microwave circuits.
7. Relatively simple and reliable fabrication sequence.
8. Extension of the technology to devices with integral antennas, antenna arrays, and microwave integrated circuits.

Future research will include parasitic element modeling, improvements in diode noise characteristics by thinning the active layer through the anode windows [13], optimization of contact pad geometry, fabrication of diodes with low doping for cryogenic operation, reactive ion etching to produce micron and submicron anodes with improved oxide window profile, and improvement of contact pad metallization for enhanced solderability.

Acknowledgements

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